

Alveo U50 Data Center Accelerator Card

User Guide

UG1371 (v1.0) August 2, 2019



Revision History

The following table shows the revision history for this document.

Section	Revision Summary
08/02/2019 Version 1.0	
Initial release	N/A

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Introduction

The Xilinx® Alveo™ U50 Data Center accelerator cards are peripheral component interconnect express (PCIe®) Gen3 x16 compliant and Gen4 x8 compatible cards featuring the Xilinx 16 nm UltraScale+™ technology. The Alveo U50 card offers 8 GB of HBM2 at 460 GB/s bandwidth to provide high-performance, adaptable acceleration for memory-bound, compute-intensive applications including database, analytics, and machine learning inference.

The following table lists the specifications for the engineering sample (ES3) and production (PQ) versions of the Alveo U50 accelerator cards.

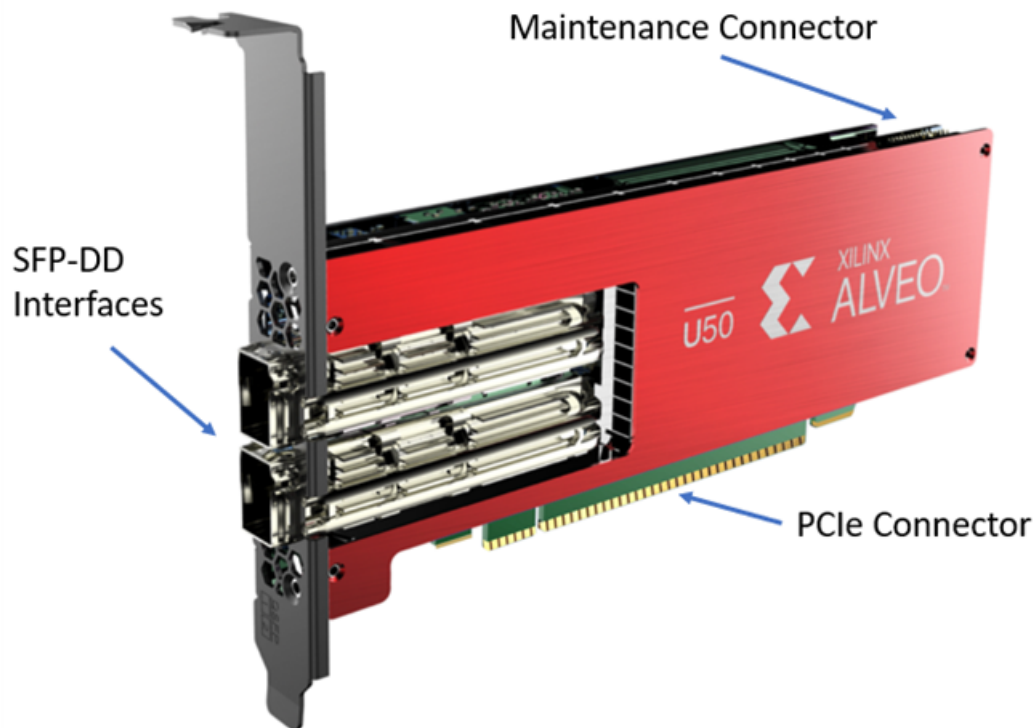
Table 1: Alveo Card Specifications

Specification	ES3 Version	PQ Version
Product SKU	A-U50DD-P00G-ES3-G	A-U50-P00G-PQ-G
Network interface	2xSFP-DD	1xQSFP
Qualified for deployment	No	Yes

The Alveo™ U50 card is available in a passive cooling configuration only and is designed for installation into a data center server where controlled air flow provides direct cooling to the card. The following figure shows the Alveo U50 ES3 accelerator card with full-height bracket installed. The card includes the following interfaces:

1. A PCI Express® card connector.
2. Two SFP-DD interfaces.
 - Note:** For production cards, only one QSFP interface is available.
3. Maintenance Connector.

Figure 1: Alveo U50 ES3 Data Center Accelerator Card



CAUTION! Alveo accelerator cards are designed to be installed into a data center server, where controlled air flow provides direct cooling. If the cooling enclosure is removed from the card and the card is powered-up, external fan cooling airflow **MUST** be applied to prevent over-temperature shut-down and possible damage to the card electronics. Removing the cooling enclosure voids the board warranty.

See [Appendix C: Additional Resources and Legal Notices](#) for references to documents, files, and resources relevant to the Alveo U50 accelerator cards.

Card Features

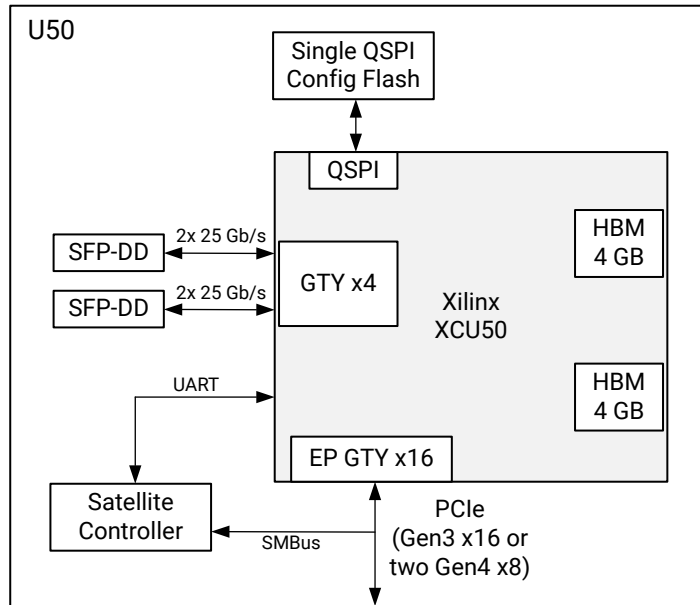
The Alveo U50 accelerator card features are listed below. Detailed information for each feature is provided in [Chapter 4: Card Component Description](#).

- UltraScale+™ XCU50 FPGA
- Two stacks of 4 gigabyte (GB) HBM memory (8 GB total)
 - 32 channels of 256 MB
 - 8 GB total providing a maximum bandwidth of 460 GB/s
- 8 GB at 460 GB/s of HBM2 memory
- One gigabit (Gb) quad SPI flash memory for configuration
- Ethernet networking interfaces
 - Two SFP-DD connectors support 4x10/25 GbE (*ES3 card*)
 - One QSFP28 connector supporting 100 GbE, 40 GbE, or 4x10/25 GbE (*PQ card*)
- JTAG and UART access through the maintenance connector
- 16-lane integrated Endpoint block for PCI Express connectivity
 - Gen3 x16 supporting to x1, x2, x4, x8, x16 lane configurations
 - Single or dual Gen4 x8
- I2C bus
- Status LEDs
- Power management with system management bus (SMBus) voltage, current, and temperature monitoring
- 75W PCIe slot power only

Block Diagram

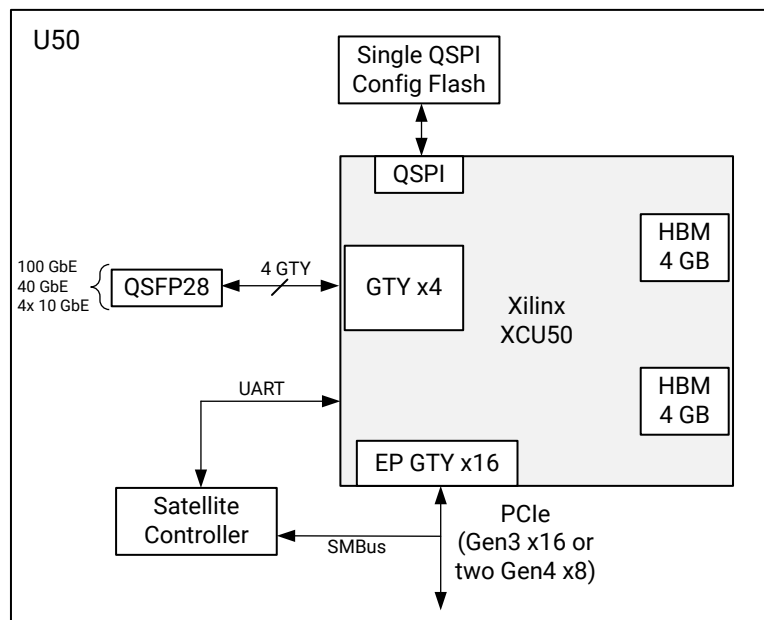
Block diagrams of the Alveo U50 card with two SFP-DD interfaces (ES3 card) and one QSFP interface (PQ card) are shown in the following figures.

Figure 2: Card Block Diagram with SFP-DD Interface



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Figure 3: Card Block Diagram with QSFP Interface

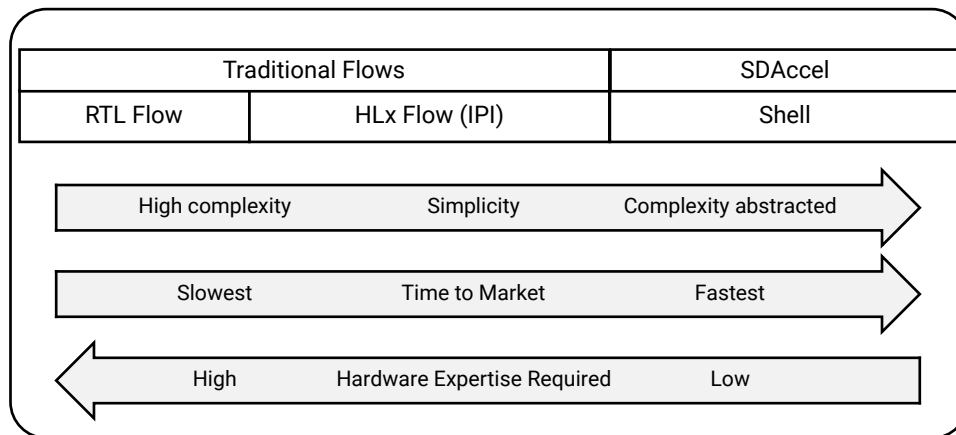


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Design Flows

The preferred optimal design flow for targeting the Alveo Data Center accelerator card uses the SDAccel™ development environment. However, traditional design flows, such as RTL or HLx are also supported using the Vivado® Design Suite tools. The following figure shows a summary of the design flows.

Figure 4: Alveo Data Center Accelerator Card Design Flows



X22272-020419

Requirements for the different design flows are listed in the following table.

Table 2: Requirements to Get Started with Alveo Data Center Accelerator Card Design Flows

	RTL Flow	HLx Flow	SDAccel
Flow documentation	UG949 ¹	UG895 ²	UG1023 ³
Vivado tools support	Board support XDC	Board support XDC	N/A
Programming the FPGA	Vivado Hardware Manager	Vivado Hardware Manager	UG1370 ⁴

Notes:

1. *UltraFast Design Methodology Guide for the Vivado Design Suite (UG949).*
2. *Vivado Design Suite User Guide: System-Level Design Entry (UG895).* See "Using the Vivado Design Suite Platform Board Flow" in Chapter 2 and Appendix A.
3. *SDAccel Environment User Guide (UG1023).*
4. *Alveo U50 Data Center Accelerator Card Installation Guide (UG1370).*

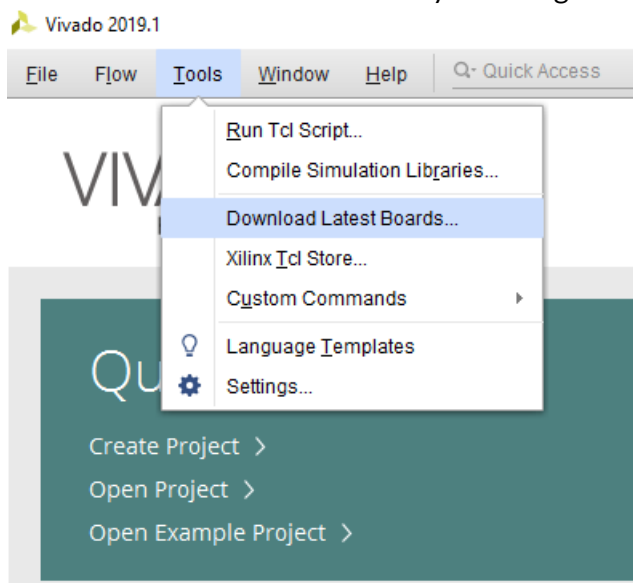
Vivado Design Flow

This section provides a starting point for expert HDL developers using the RTL flows, or developers who want to customize in HLx beyond the standard support in the Vivado® tools.

Board Support Files for the Alveo U50 Card

Prior to creating an RTL project based on the Alveo™ U50 card, update the board support repository to include the Alveo U50 card by following the steps listed below.

1. Launch Vivado tools.
2. Download the latest board files by selecting **Tools** → **Download Latest Boards...**

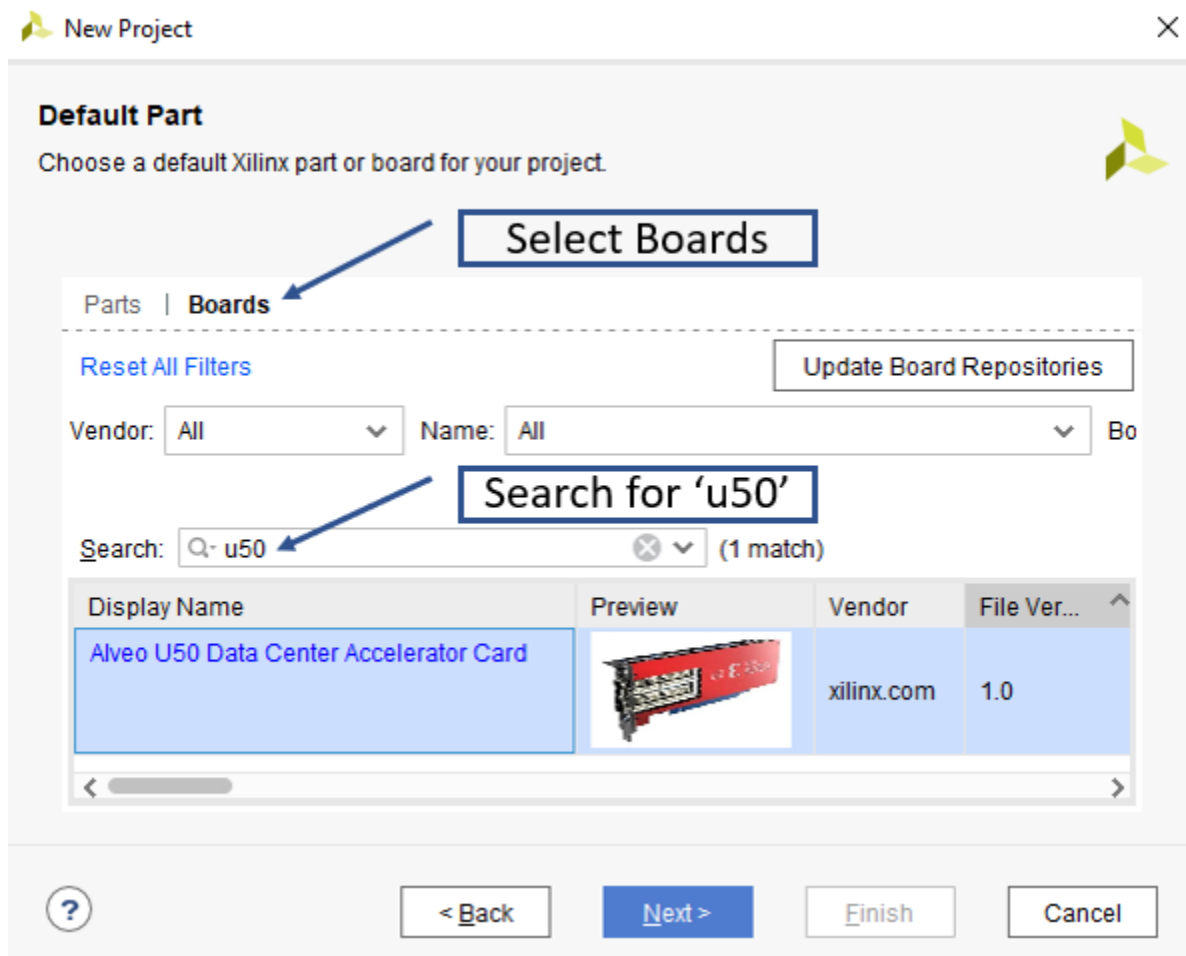


3. Click **Download** in the Download Latest Boards dialog box. This will download all the latest board support files including those for the Alveo U50 card. The download may take several minutes to complete.

Creating an RTL Project Based on the U50 Board File

For designers using RTL flow, use the following steps to create an RTL project using the U50 board file.

1. Launch Vivado tools.
2. Create a new project by clicking on **File** → **Project** → **New**. Click **Next**.
3. Add a project name and click **Next**.
4. Select **RTL Project** as the Project Type and click **Next**.
5. Within the Default Part window, select **Boards** and enter **u50** in the search tab. Select the **U50** card and click **Next** as shown in the following figure.



This will create a new RTL project based on the Alveo U50 accelerator card.

Creating an MCS File and Programming the Alveo Card

For custom RTL flow, this section outlines the procedures to do the following:

- Create an MCS file (PROM Image)
- Flash program through the maintenance connector

Create an MCS File (PROM Image)

To ensure that the PROM image is successfully loaded onto the Alveo accelerator card at power on, the starting address must be set to `0x01002000` and the interface set to `spix4` when creating the MCS file. Details on adding this to the MCS file can be found in the *UltraScale Architecture Configuration User Guide* ([UG570](#)).

The Alveo accelerator card's Quad SPI configuration flash memory contains a protected region, with the factory base image at the `0x00000000` address space. This base image points to the customer programmable region at a `0x01002000` address space offset.

In addition, the following code must be placed in the project XDC file to correctly configure the MCS file.

```
# Bitstream Configuration
# -----
set_property CONFIG_VOLTAGE 1.8 [current_design]
set_property BITSTREAM.CONFIG.CONFIGFALLBACK Enable [current_design]
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property CONFIG_MODE SPIx4 [current_design]
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 85.0 [current_design]
set_property BITSTREAM.CONFIG.EXTMASTERCLK_EN disable [current_design]
set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN Pullup [current_design]
set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR Yes [current_design]
# -----
```

Program the Alveo Card through the Maintenance Connector

After the MCS file is created, use the following steps to flash the Alveo Data Center accelerator card using the Vivado hardware manager through the debug and maintenance board (DMB). Details on connecting to the Alveo card through the maintenance connector are provided in *Alveo U50 Debug and Maintenance Board User Guide* ([UG1377](#)). Detailed steps for programming the FPGA device are outlined in the chapter *Programming the FPGA Device* in the *Vivado Design Suite User Guide: Programming and Debugging* ([UG908](#)).



RECOMMENDED: *Programming through JTAG maintenance port must be from a separate machine to avoid PCIe downlink causing the server to reboot during programming. Alternatively, the PCIe link can be manually disabled through software and rescanned after programming is complete.*

1. Connect to the Alveo U50 Data Center accelerator card using the Vivado hardware manager through the DMB.
2. Select **Add Configuration Device** and select the mt25qu01g-spi-x1_x2_x4 part.
3. Select **Program the Configuration Memory Device** on the target.
 - a. Select the MCS file target.
 - b. Select **Configuration File Only**.
 - c. Click **OK**.
4. After programming has completed, disconnect the card in the hardware manager, and disconnect the USB cable from the Alveo accelerator card.
5. Perform a cold reboot on the host machine to complete the card update.



IMPORTANT! *If you are switching between an Alveo Data Center accelerator card shell and a custom design, revert the card to the golden image before loading an alternate image into the PROM. See Alveo U50 Data Center Accelerator Card Installation Guide ([UG1370](#)) for more information.*

Card Installation and Configuration

Electrostatic Discharge Caution



CAUTION! ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.

To prevent ESD damage:

- Use an ESD wrist or ankle strap and ensure that it makes skin contact. Connect the equipment end of the strap to an unpainted metal surface on the chassis.
 - Avoid touching the adapter against your clothing. The wrist strap protects components from ESD on the body only.
 - Handle the adapter by its bracket or edges only. Avoid touching the printed circuit board or the connectors.
 - Put the adapter down only on an antistatic surface such as the bag supplied in your kit.
 - If you are returning the adapter to Xilinx Product Support, place it back in its antistatic bag immediately.
-

Installing Alveo Data Center Accelerator Cards in Server Chassis

For hardware and software installation procedures, see the *Alveo U50 Data Center Accelerator Card Installation Guide* ([UG1370](#)).

Because each server or PC vendor's hardware is different, for physical board installation guidance, see the manufacturer's PCI Express[®] board installation instructions.

FPGA Configuration

The Alveo U50 accelerator card supports two UltraScale+™ FPGA configuration modes:

- Quad SPI flash memory
- JTAG (through maintenance port)

The FPGA bank 0 mode pins are hardwired to M[2:0] = 001 master SPI mode with pull-up/down resistors.

At power up, the FPGA is configured by the QSPI NOR flash device (Micron MT25QU01GBB8E12-0SIT) with the FPGA_CCLK operating at a clock rate of up to 125 MHz (EMCCLK) using the master serial configuration mode.

If the JTAG cable is plugged in, QSPI configuration might not occur. JTAG mode is always available independent of the mode pin settings.

For complete details on configuring the FPGA, see the *UltraScale Architecture Configuration User Guide* ([UG570](#)).

Table 3: Configuration Modes

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master SPI	001	x1, x2, x4	FPGA output
JTAG	Not applicable - JTAG overrides	x1	Not applicable

Card Component Description

This chapter provides a functional description of the components of the Alveo™ U50 Data Center accelerator card.

UltraScale+ FPGA

The Alveo U50 accelerator card is populated with the 16 nm UltraScale+™ XCU50 FPGA.

This UltraScale+ HBM device incorporates two 4 GB high-bandwidth memory (HBM) stacks adjacent to the device die. Using SSI technology, the device communicates to the HBM stacks through memory controllers that connect through the silicon interposer at the bottom of the device. Each XCU50 FPGA contains two 4 GB HBM stacks, resulting in up to 8 GB of HBM per device. The device includes 32 HBM AXI interfaces used to communicate with the HBM. The flexible addressing feature that is provided by a built-in switch allows for any of the 32 HBM AXI interfaces to access any memory address on either one or both of the HBM stacks. This flexible connection between the device and the HBM stacks is helpful for floorplanning and timing closure.

Quad SPI Flash Memory

The Quad SPI device provides 1 Gb of nonvolatile storage.

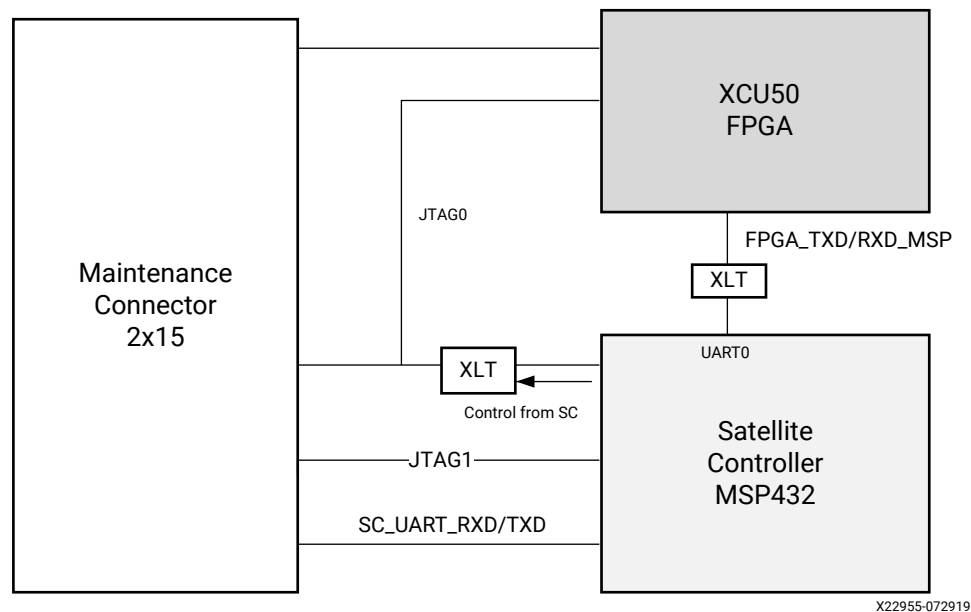
- Part number: MT25QU01G BBB8E12-0AAT (Micron)
- Supply voltage: 1.8V
- Datapath width: 4 bits
- Data rate: variable

For configuration details, see the *UltraScale Architecture Configuration User Guide* ([UG570](#)). The detailed FPGA connections for the feature described in this section are documented in the Alveo U50 accelerator card XDC file, referenced in [Appendix A: Xilinx Design Constraints \(XDC\) File](#).

Maintenance Connector Interface

The Alveo U50 accelerator card provides access to the FPGA through the JTAG interface using a debug and maintenance board (DMB) connected to the 30-pin maintenance connector. The connector pinout supports three UART debug interfaces: PMBus, FPGA JTAG, and satellite controller JTAG. The following figure shows the maintenance connector interface. For more information, see *Alveo U50 Debug and Maintenance Board User Guide* ([UG1377](#)).

Figure 5: Maintenance Connector



PCI Express Endpoint

The Alveo U50 accelerator card implements a 16-lane PCI Express edge connector that performs data transfers at the rate of 2.5 giga-transfers per second (GT/s) for Gen1, 5.0 GT/s for Gen2, 8.0 GT/s for Gen3 applications, and 16.0 GT/s for Gen4 applications.

The detailed FPGA connections for this feature are documented in the Alveo U50 accelerator card Xilinx Design Constraints (XDC) file, referenced in [Appendix A: Xilinx Design Constraints \(XDC\) File](#).

SFP-DD Module Connectors

The Alveo U50 accelerator cards host two small form-factor pluggable (SFP-DD) connectors that accept an array of optical modules. Each connector is housed within a single cage assembly and are accessible through the I2C interface.

Access from the FPGA to SFP-DD modules and support for miscellaneous SFP-DD signals is provided through the satellite controller. For more information about the SFP-DD module, see [SFP-DD Specification](#).

- MGTREFCLK0 is from SI5394 with programmable output frequencies
- Maximum SFP-DD power is 3.5W per port
- The target for SFP-DD channel length is 4 inches maximum

Detailed FPGA connections for this feature are documented in the Alveo U50 accelerator card XDC file, referenced in [Appendix A: Xilinx Design Constraints \(XDC\) File](#).

I2C Bus

The Alveo U50 accelerator cards implement an I2C bus network.

Status LEDs

The U50 has two set of LEDs:

1. Card status LEDs
2. Ethernet status LEDs

Card status LEDs are visible through a cutout in the PCIe end bracket and are defined in the following table. Production cards will not have board status LEDs.

Table 4: Card Status LEDs

Reference Designator	Description
DS1	FPGA done when blue
DS2	System healthy when green ¹
DS3	Warning or alarm when orange ¹

Table 4: Card Status LEDs (cont'd)

Reference Designator	Description
DS4	Power fault when red.

Notes:

1. Functionality is not yet defined.

Ethernet status LEDs are located on the top-left, front panel above the SFP-DD modules. The LED definitions are given in the following table.

Table 5: Ethernet Status LEDs

Reference Designator	Description
SFPDD_0_ACTIVITY_LED	Green SFP-DD0 ¹
SFPDD_0_STATUS_LEDG	Green SFP-DD0 ¹
SFPDD_0_STATUS_LEDY	Yellow SFP-DD0 ¹
SFPDD_1_ACTIVITY_LED	Green SFP-DD1 ¹
SFPDD_1_STATUS_LEDG	Green SFP-DD1 ¹
SFPDD_1_STATUS_LEDY	Yellow SFP-DD1 ¹

Notes:

1. Functionality is not yet defined.

Card Power System

Limited power system telemetry is available through the I2C IP. I2C IP is instantiated during the FPGA design process which begins after the Alveo Data Center accelerator card is selected from the Vivado Design Suite Boards tab. Refer to [Design Flows](#) for more information.

Xilinx Design Constraints (XDC) File

RTL users can reference the *Vivado Design Suite User Guide: Using Constraints (UG903)* for more information. The Alveo accelerator card XDC files are available for download from their respective websites along with this user guide.

Note: Bitstream constraints are not available for download because they are user-generated.

Regulatory and Compliance Information

This product is designed and tested to conform to the European Union directives and standards described in this section.

CE Directives

2014/35/EC, *Low Voltage Directive (LVD)*

2014/30/EC, *Electromagnetic Compatibility (EMC) Directive*

CE Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

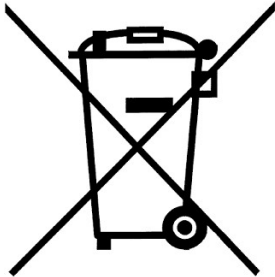
Electromagnetic Compatibility

EN:55032:2015, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN:55024:2015, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

Compliance Markings



In August of 2005, the European Union (EU) implemented the EU Waste Electrical and Electronic Equipment (WEEE) Directive 2002/96/EC and later the WEEE Recast Directive 2012/19/EU. These directives require Producers of electronic and electrical equipment (EEE) to manage and finance the collection, reuse, recycling and to appropriately treat WEEE that the Producer places on the EU market after August 13, 2005. The goal of this directive is to minimize the volume of electrical and electronic waste disposal and to encourage re-use and recycling at the end of life.

Xilinx has met its national obligations to the EU WEEE Directive by registering in those countries to which Xilinx is an importer. Xilinx has also elected to join WEEE Compliance Schemes in some countries to help manage customer returns at end-of-life.

If you have purchased Xilinx-branded electrical or electronic products in the EU and are intending to discard these products at the end of their useful life, please do not dispose of them with your other household or municipal waste. Xilinx has labeled its branded electronic products with the WEEE Symbol to alert our customers that products bearing this label should not be disposed of in a landfill or with municipal or household waste in the EU.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see [Xilinx Support](#).

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. DocNav is installed with the SDSoc™ and SDAccel™ development environments. To open it:

- On Windows, select **Start** → **All Programs** → **Xilinx Design Tools** → **DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the [Design Hubs](#) page.

Note: For more information on DocNav, see the [Documentation Navigator](#) page on the Xilinx website.

References

Product Websites

The most up-to-date information related to the Alveo™ U50 card and documentation is available on the following websites:

[Alveo U50 Data Center Accelerator Card](#)

Supplemental Documents

The following Xilinx document provide supplemental material useful with this guide.

- *UltraFast Design Methodology Guide for the Vivado Design Suite* ([UG949](#))
- *Vivado Design Suite User Guide: System-Level Design Entry* ([UG895](#))
- *Getting Started with Alveo Data Center Accelerator Cards* ([UG1301](#))
- *Alveo U50 Data Center Accelerator Card Installation Guide* ([UG1370](#))
- *Alveo U50 Debug and Maintenance Board User Guide* ([UG1377](#))
- *UltraScale Architecture Configuration User Guide* ([UG570](#))
- *Vivado Design Suite User Guide: Programming and Debugging* ([UG908](#))
- *Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics* ([DS923](#))
- *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* ([PG150](#))
- *Vivado Design Suite User Guide: Using Constraints* ([UG903](#))
- *UltraScale Architecture PCB Design User Guide* ([UG583](#))

Additional Links

The following links provide supplemental material useful with this guide.

- Xilinx, Inc: <https://www.xilinx.com>
- Micron Technology: <http://www.micron.com>
- *Si5394 Data Sheet*: <https://www.silabs.com/documents/public/data-sheets/si5395-94-92-a-datasheet.pdf>
- Future Technology Devices International, Ltd.: <http://www.ftdichip.com>
(FT4232HQ)
- SFP-DD module: [SFP-DD Specification](#)

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